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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/932,086	08/17/2001	Georg Farkas	CH 000018	5457

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EXAMINER	
ENG, MARSHALL S	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 01/28/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/932,086	FARKAS ET AL.	
	Examiner	Art Unit	
	Marshall S Eng	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 August 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Priority

1.1 Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

1.2 A statement claiming priority the previously filed foreign document should also be placed in the first line of the Specifications listing the country of filing, filing date, and foreign application number.

Information Disclosure Statement

2.1 The information disclosure statement filed 16 October 2003 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. It has been placed in the application file, but the information referred to therein has not been considered.

Drawings

3.1 Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4.1 The disclosure is objected to because of the following informalities: the layout of the specifications should be amended so as to include section headings (i.e. Background of the invention (Field of the invention and Description of related art), Brief summary of the invention, Brief Description of the diagrams/drawings, Detailed description of the invention, etc.).

4.2 The disclosure is further objected to because of the following informalities: the word "in" in the phrase "consists in" on line 6 of page 1 should be changed to "of."

4.3 The disclosure is further objected to because of the following informalities: one of the words "necessitate" or "require" on line 17 of page 1 should be removed because they both mean the same thing.

4.4 Claims 1-9 are objected to because of the following informalities: since the claims clearly describe two different embodiments (Figures 3 and 4), the two figures should not share common reference numbers if the reference numbers are to be used.

4.5 Claims 1-9 are further objected to because of the following informalities: the claims include information with brackets/parentheses and is therefore not given patentable weight.

4.6 Claims 1-9 are further objected to because of the following informalities: indentation of plural limitations is required in a claim.

4.7 Claim 5 is further objected to because of the following informalities: the word "a" on line 1 should be "as."

Appropriate corrections are required.

Claim Rejections - 35 USC § 103

5.1 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

5.2 This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5.3 Claim(s) 1-4 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art 'Specifications' (hereinafter Specs).

As per claim 1,

Specs substantially teaches of testing integrated circuits using a test system (1 of Figure 1) and a logic component/block (8 of figure 1) that is included in the IC to be tested, see lines 5-10 of page 4 where Figure 1 is discussed and disclosed as being in accordance with the present state of the art.

Further, Specs teaches of using test vector pattern generators to generate test vectors, see lines 10-25 of page 1, as widely used in the art. Still further, Specs

teaches that using test vector pattern generators are an alternative to loading the test vectors into large test memories.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a test vector pattern generator in an embodiment as described by Specs in Figure 1 and lines 5-10 of page 4. One of ordinary skill in the art would be motivated to use a test vector pattern generator in the embodiment so as to prevent from having to use a large test memory as suggested by Specs in lines 10-14 of page 1. By replacing the large test memory with a test pattern generator, one of ordinary skill in the art would save IC space and cost by not having to implement the test vectors in large test memories.

As per claim 2,

Specs further teaches of an IC including a test analysis unit (5 of Figure 2) for compressing response vectors and a test control block (6 of Figure 1 and 2) for controlling the test procedure. Since both Figures 1 and 2 are known descriptions of the art, it would have been obvious to one of ordinary skill to combine the integrated test analysis unit of Figure 2 into the IC of Figure 1. Since both embodiments are known in the art, it would have been an obvious step to one of ordinary skill in the art to include the analysis unit. Further, one of ordinary skill would have known that by implementing a test analysis unit on chip, it would allow the system to only be required to send the signature (i.e. compressed responses) instead of all of the test response vectors. Because of the compression of the responses into a single signature, less data would

have to be transferred (i.e. single signature vs. all of the response vectors) thereby increasing the speed at which an IC is tested.

As per claim 3,

Test vectors are created so as to test an IC (or DUT). Therefore, it would have been obvious to one of ordinary skill in the art to generate test vectors that are intended to be transferred to the IC to be tested. The vectors are created so as to be applied to an IC/memory/DUT and therefore are always intended to be transferred to the IC/memory/DUT to be tested.

As per claim 4,

Specs further teaches that response analysis creates a checksum by compressing the response vectors into a single signature/checksum, see lines 20-25 of page 1, lines12-17 of page 4, and lines 7-8 of page 5 where it is disclosed that response analysis units compresses responses into signature or checksum. The examiner is interpreting a compressed compressed to be equivalent to a signature.

5.4 Claim(s) 5-9 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art 'Specifications' (hereinafter Specs) in view of Derwent Abstract ACC-NO 1988-141950 (hereinafter Dias).

As per claim 5,

Specs substantially teaches, as combined above in claim 1, the limitations of claim 5.

Specs, however, does not teach of using a programmable test vector generator that includes an ALU (i.e. processor).

Dias in an analogous art, teaches of using a processor to feed a test vector generator with the required characteristics of the system. The processor is used to determine the test vectors used, see page 2 of Dias under "Basic-Abstract."

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the programmable test vector generator of Dias instead of the test vector generator of Specs in the arrangement of Specs. One of ordinary skill would have been motivated to do so by the suggestion of Dias that by using processor to help determine the test vectors used, a smaller number of vectors are required while being able to detect all faults (i.e. maintain coverage) in a circuit, see page 2 of Dias under "Equivalent-Abstract."

As per claim 6,

Specs substantially teaches, as combined above in claims 1-4, of a test vector generator in a test system that generates test vectors, see lines 10-25 of page 1, that are transferred to an IC that includes a logic component/block, see Figure 1 or 2. Specs further teaches of compressing the responses in an analysis unit and of evaluating the compressed responses in the test system, see lines 20-25 of page 1, lines 12-17 of page 4, and lines 7-8 of page 5.

Specs does not teach of using a programmable test vector generator.

Dias in an analogous art, teaches of using a processor to feed a test vector generator with the required characteristics of the system. The processor is used to determine the test vectors used, see page 2 of Dias under "Basic-Abstract."

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the programmable test vector generator of Dias instead of the test vector generator of Specs in the arrangement of Specs. One of ordinary skill would have been motivated to do so by the suggestion of Dias that by using processor to help determine the test vectors used, a smaller number of vectors are required while being able to detect all faults (i.e. maintain coverage) in a circuit, see page 2 of Dias under "Equivalent-Abstract."

As per claim 7,

Specs substantially teaches, as combined above in claim 2, of an IC with an analysis unit and a control block (see Figures 1 and 2), where the IC receives generated test vectors from a test vector generator in a test system that generates test vectors that are transferred to an IC, see lines 10-25 of page 1. Specs further teaches of the IC generating response vectors that are compressed in the analysis unit that is under control of the control block, see lines 5-10 of page 4.

Specs does not teach of using a programmable test vector generator.

Dias in an analogous art, teaches of using a processor to feed a test vector generator with the required characteristics of the system. The processor is used to determine the test vectors used, see page 2 of Dias under "Basic-Abstract."

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the programmable test vector generator of Dias instead of the test vector generator of Specs in the arrangement of Specs. One of ordinary skill would have been motivated to do so by the suggestion of Dias that by

using processor to help determine the test vectors used, a smaller number of vectors are required while being able to detect all faults (i.e. maintain coverage) in a circuit, see page 2 of Dias under "Equivalent-Abstract."

As per claim 8,

Specs substantially teaches, as combined above in claims 1-4, of a test system that includes a test pattern generator that generates test vectors that are to be transferred/applied to an IC to be tested, see lines 10-25 of page 1 and Figure 1, with the test system capable of receiving and evaluating the test response vectors, see lines 10-15 of page 4 specifically where the test response vectors are transferred via the connectors 11 (to the test system).

The response analyzer of Figure 2 clearly receives the test response vectors. Further, Specs teaches that analysis units compress the responses into a signature, therefore the analysis unit must receive and evaluate the vectors, see lines 20-25 of page 1.

As per claim 9,

Specs further teaches that response analysis creates a checksum by compressing the response vectors into a single signature/checksum, see lines 20-25 of page 1, lines12-17 of page 4, and lines 7-8 of page 5 where it is disclosed that response analysis units compresses responses into signature or checksum. The examiner is interpreting a compressed checksum to be equivalent to a signature.

Specs further teaches of an IC including a test analysis unit (5 of Figure 2) for compressing response vectors and a test control block (6 of Figure 1 and 2) for

controlling the test procedure. Since both Figures 1 and 2 are known descriptions of the art, it would have been obvious to one of ordinary skill to combine the integrated test analysis unit of Figure 2 into the IC of Figure 1. Since both embodiments are known in the art, it would have been an obvious step to one of ordinary skill in the art to include the analysis unit. Further, one of ordinary skill would have known that by implementing a test analysis unit on chip, it would allow the system to only be required to send the signature (i.e. compressed responses) instead of all of the test response vectors. Because of the compression of the responses into a single signature, less data would have to be transferred (i.e. single signature vs. all of the response vectors) thereby increasing the speed at which an IC is tested.

Conclusion

6.1 The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Dias et al. U.S. Patent No. 5,010,552

b. Komonytsky U.S. Patent No. 4,519,078

c. Salik U.S. Patent No. 4,672,610

6.2 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marshall S Eng whose telephone number is (703) 305-4638. The examiner can normally be reached on M-Th, 9 am to 5:30 pm and F, 9 am to 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

mse

Guy J. Lamarre
for

Albert DeCady
Primary Examiner